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Question: 4. Write a test bench program for 4-bit Full Adder / Subtractor u...



4. Write a test bench program for 4-bit Full Adder / Subtractor using the given truth table and verify its Verilog code for 4-bit Full Adder / Subtractor.

4-bit Full Adder / Subtractor						
Carry-in	Inputs		Outputs			
	A	B	A+B	Carry out	A-B	Borrow out
0	0001	0101				
1	0001	0101				
0	1001	0001				
1	1001	0000				
0	0110	0010				
1	0110	0010				
0	0001	0111				
1	0001	0111				
0	1111	1111				
1	1111	1111				

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Expert Answer



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Test bench for 4-bit Adder/subtractor module

timescale 1ns/1ps

module addorsubtract_4bit_tb;

inputs

reg [3:0] A;

reg [3:0] B;

reg cin;

//outputs

wire [3:0] sum, [3:0] borrow;

wire carryout, borrowout;

// Temporary looping variable:

reg [3:0] i = 4'd0;

// Instantiate the unit under Test (UUT)

add_subtract_4bit uut (A1, A2, A3, A4, B1, B2,

• A1(A[0]), • A2(A[1]), • A3(A[2]), • A4(A[3]),

• B1(B[0]), • B2(B[1]), • B3(B[2]), • B4(B[3]), • cin, cin,

• S1(sum[0]), • S2(sum[1]), • S3(sum[2]), • S4(sum[3]),

• cout(carryout), • B01(borrow[0]), • B02(borrow[1]),

• B03(borrow[2]), • B04(borrow[3]), • Bout(borrowout)

);

// A1, A2, A3, A4, B1, B2, B3, B4 = A, B inputs

// cin, cin

// S1, S2, S3, S4 = sum[0:3], B01, B02, B03, B04 = borrow[0:3],

cout, carryout, Bout = borrowout

initial begin

A = 4'b0;

B = 4'b0;

cin = 1'b0;

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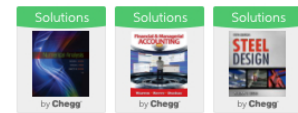
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```

wait 100ns for global reset
#100;
// stimulus
for i = 0; i < 16; i = i + 1'b1 begin
    { A, B, cin } = { A, B, cin } + 1'b1;
end
#20;
end
// Above stimulus covers all input combinations.
endmodule

```

If you want individual stimulus after #100 in above code.
 ↳ remove temporary looping declaration.

```

A = 4'b0001;
B = 4'b0101;
cin = 0;
#20
cin = 1;
#20
#50 on.

```

Repeat above fragment for all other input stimulus. Write \$finish after all stimulus to end simulation.

Mistake: change limit from 16 to 31 in for loop.

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Q: 4. Write a test bench program for 4-bit Full Adder / Subtractor using the given truth table and verify its Verilog code for 4-bit Full Adder / Subtractor. Inputs 4-bit Full Adder / Subtractor Outputs A+B Carry A-B Carry-in A. Borrow out out 0 0001 0101 0001 0101 1001 0001 1001 0000 0110 0010 0110 0010 0001 0111 0001 0111 11111111 1111 1111

A: See answer  100% (1 rating)

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7- Analyze the stability & causality for the following LTI systems: a. $h(t) = e^{-3t}u(t-1)$ b. $h(t) = e^{2t}u(t-1)$ c. $h(t) = u(t-1) - 2u(t-3) + u(t-4)$ d. $h(t) = u(t-1) - 2u(t-3) + u(t-4)$

7- Analyze the stability & causality for the following LTI systems:
 a. $h(t) = e^{-3t}u(t-1)$
 b. $h(t) = e^{2t}u(t-1)$
 c. $h(t) = u(t-1) - 2u(t-3) + u(t-4)$
 d. $h(t) = u(t-1) - 2u(t-3) + 2u(t-4)$

See answer

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A: See answer  100% (1 rating)

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A: See answer  100% (2 ratings)

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