WORLD'S #1 ACADEMIC OUTLINE

EST 1991 QuickStudy ACADEMIC

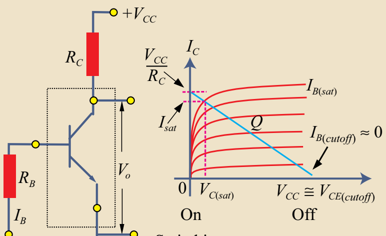
# Electronics 2

## Fundamentals of Electronic Devices & Basic Electronic Circuits

## Transistor as a Switch

*Fig. 1*

Transistor as a Switch

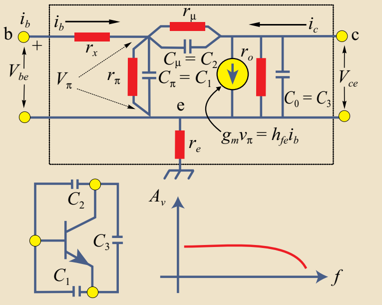


Switching states:
Low voltage and high current:
$I_B = I_{B(sat)}$ $V_o = V_{CE(sat)} \cong 1$ volt
High voltage and low current:
$I_B \cong 0$ $V_{CE(cutoff)} \cong V_{CC}$

- Transistor capacitances (*fig. 2*):
  - $C_\mu$: Junction capacitance at **CBJ** due to the depletion layer (≈ **10 pf**)
  - $C_\pi$: Diffusion capacitance at **EBJ** due to storage in the base (≈ **100 – 200 pf**)
  - Parasitic/stray capacitance due to loads and packaging
  - β cutoff frequency: $f_T \triangleq \frac{\beta}{2\pi r_\pi (C + C_\pi)} = \beta f_\beta$
  - α cutoff frequency: $(f\alpha) = \frac{f\beta}{(1 - \alpha)}$

*Fig. 2*

Transistor Capacitances



Capacitance effect: High frequency gain is reduced

## Differential Amplifiers

$$|V_{out}| = \left[V_{in1}\frac{R_{L1}\beta}{h_{ie}} - V_{in2}\frac{R_{L2}\beta}{h_{ie}}\right]$$

- If $R_{L1} = R_{L2}$, $V_{out} = G(V_{in1} - V_{in2})$ ⇒ Useful in amplifying differential signals from bridge circuits (*fig. 4*)
- The signal at $V_{in1}$ drives the base current at the transistor.
- This proportionately increases the collector current of transistor 1 and the voltage across $R_{L1}$ increases; or, the voltage output $V_o$ decreases (since $V_o + V_{RL1} = V_{CC}$ = constant). Thus, $V_{in1}$ and $V_o$ are phase opposed. We assume that $V_{in1} = 0$. Hence, the signal at $V_{in2}$ drives a base current at transistor 2 and increases the collector current of 2. The emitter potential $V_K$ is brute forced at $(V_{B1} - 0.7)$ volts.
- Therefore, increases in the emitter current of transistor 2 should correspondingly reduce the emitter (and thus the collector) current of transistor 1 such that the potential across $R_K$, $V_K$ remains as a constant brute-forced value. Thus, decreases in the collector current in transistor 1 should reduce the voltage drop across $R_{L2}$. Or, the output voltage $V_o$ should increase. Thus, increases in the input signal at transistor 2 ($V_{in2}$) increase the output voltage.
  - $V_{in1}$ → Inverting input signal
  - $V_{in2}$ → Noninverting input signal
  - $V_{o\mu}(V_{in2} - V_{in1})$
- A **basic differential amplifier** enables the mathematical difference operation and can be modified to perform operations including addition, integration, and differentiation. Thus, it is designated as an **operational amplifier (op-amp)**.

*Fig. 3*

Differential Amplifiers

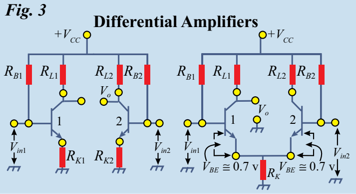


*Fig. 4*

Bridge Circuit

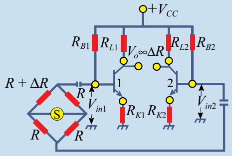
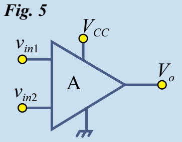


*Fig. 5*

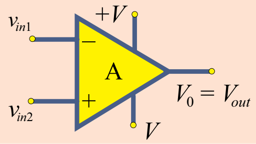


## Operational Amplifiers

### Definitions

- A basic differential amplifier (*see* **Differential Amplifiers**, above right) is designated as an operational amplifier (op-amp).
- An op-amp essentially represents a high-gain electronic circuit that is intended to amplify the difference in the signal voltages applied to its two input terminals, i.e., inverting (–) and noninverting (+) inputs (*fig. 6*).

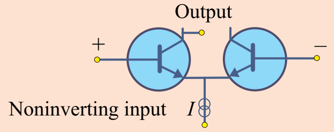
*Fig. 6*



- In simple form (*fig. 7*), an op-amp constitutes a differential amplifier that is composed of, for example, a pair of BJTs driven by a constant current source (*I*). JFETs and MOSFETs can be used as differential pairs.

*Fig. 7*

Differential Pair



### Ideal Op-Amp Characteristics

- Nominal voltage gain, $A \to \infty$
- Input impedance (at both inputs), $Z_{in} \to \infty$
- Output impedance, $Z_0 \to 0$
- Both transistors are identical.
- $v_0 = -Av_{in1} = Av_{in2}$; or, if $v_{in1} = v_{in2}$, $v_0 = 0$
- Bandwidth ($BW$) → ∞
  - With bipolar transistors, it is potentially difficult to achieve an extremely high-input impedance.
  - JFETs and MOSFETs provide high-input impedance capabilities.

### Op-Amp Operational Parameters

With respect to typical inverting (*fig. 8*) and noninverting (*fig. 9*) modes of operational characteristics:

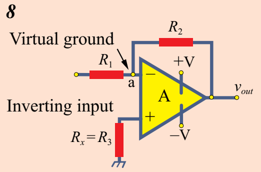
- **Input bias current:** This is the emitter current in the differential amplifier for the active region operation of the pair of BJTs (e.g., **0.05 μA** for a 741 op-amp) that comes through $R_2$ such that $v_{out} = (0.05 \times 10^{-6} \times R_2)$ volts. This can be sufficiently high to saturate the output. Saturation is overcome via introducing $R_x = R_1 \parallel R_2$ and adjusting it to compensate for the input offset current due to any dissimilarities in the differential-pair configuration (*fig. 8*).
- **Input offset voltage** (≈ **±60 mV**)**:** It is required at the input as a counter voltage to offset the finite unbalance voltage due to unequal current flowing through the differential-pair devices in the op-amp, and thus the balancing yields zero output voltage.
- **CMRR:** When the op-amp is ideally balanced at the input, the output voltage = **0** (i.e., $v_{in1} = v_{in2}$), and the circuit can reject common-mode signals due to its common-mode gain $(A_c) = 0$. With respect to differential-mode signals $(v_{in1} - v_{in2})$, the gain $(A_d) \to \infty$. The ratio is $A_d/A_c$ **common-mode rejection ratio** (CMRR). In practical op-amps, $A_c > 0$ and $A_d < \infty$; or, CMRR is finite and indicates the extent of balance in the op-amp (a figure of merit parameter).
- **Output voltage swing:** This corresponds to the peak output swing with reference to zero at the output. It is limited by the power supply voltages used (≈ **80%** of power supply voltage ±**V**).
- **Input voltage swing:** Input common-mode voltage swing is limited by the saturation of the differential amplifier at the input (≈ **30%** of power supply voltage ±**V**).
- **Slew rate:** Maximum rate at which the output voltage can change (volts/microsecond). In ideal op-amps, slew-rate → ∞.
- **Other parameters:**
  - Bandwidth
  - Maximum output current available when the output terminal is set to ground
  - **PSRR:** Power supply rejection ratio, or the change in input offset voltage to the corresponding change in one of the power supply voltages (±**V**). Ideally, **PSRR = 0**; in practice, it corresponds to the order of a few μ**V/V**.

### Frequency Roll-Off

The fall-off of the voltage gain at high frequencies. This is indicated by the gain-bandwidth product. Roll-off to higher frequencies is achieved via frequency compensation.

### Inverting Amplifier (Virtual Ground Amplifier)

*Fig. 8*



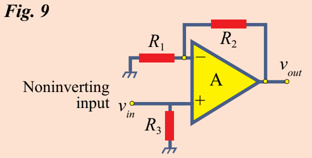
- Output impedance with feedback ≅

$$\frac{\text{Output impedance of the op-amp} \times \text{Closed-loop gain}}{\text{Open-loop gain}}$$

- Node **a** is almost at ground potential.
- Closed-loop voltage gain = $\frac{v_{out}}{v_{in}} = \frac{-R_2}{R_1}$
- Input impedance = $R_1$ and output impedance = $R_o$

### Noninverting Amplifier

*Fig. 9*

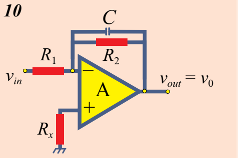


$$A_V = 1 + \frac{R_2}{R_1}$$

$Z_{in} = R_3$ and $Z_{out}$ → Low

### Integrator (Low-Pass Filter)

*Fig. 10*



- $R_2$: Provides negative feedback for low-output impedance needs although it distorts the output

$$\frac{dv_0}{dt} = -\frac{v_{in}}{R_1 C} \quad v_0 = -\left(\frac{1}{R_1 C}\right) \times \int v_{in} dt$$

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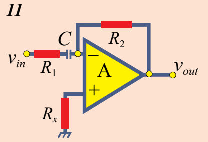
## Differentiator (High-Pass Filter)

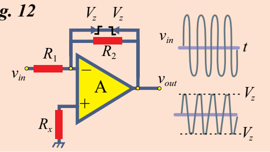
*Fig. 11*



Inverse operation of the integrator circuit

## Level Clamping

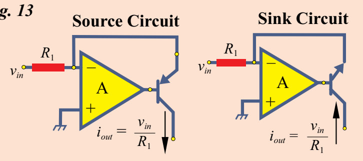
*Fig. 12*



The output is clamped to zener voltage $V_z$.

## Linear Voltage-to-Current Converters

*Fig. 13*

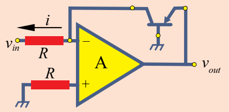


Source Circuit

Sink Circuit

## Logarithmic Amplifier

*Fig. 14*

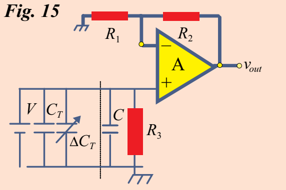


- $I_B$ : Reverse saturation current of EB junction
- α : Transistor α
- $k_B$: Boltzmann constant

$$v_{out} = \frac{k_B T}{q} ln\left(\frac{v_{in}}{\alpha I_B R}\right)$$

## Charge Amplifier

*Fig. 15*



- Input (from a capacitive transducer):

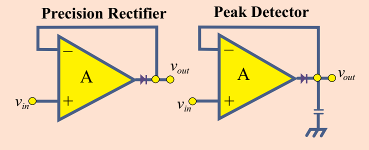
$$v_{in} = V\frac{\Delta C_T}{C}$$

- $C_T$: Nominal capacitance of the transducer charge by voltage $V$

$$v_{out} = v_{in}\left(1+\frac{R_2}{R_1}\right)$$

## Precision Rectifier & Peak Detector

*Fig. 16*

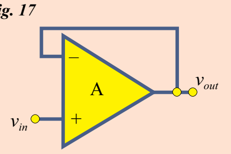


Precision Rectifier

Peak Detector

## Voltage Follower (Unity-Gain Amplifier)

*Fig. 17*



$$Z_{in} = A \times [R_{in(Device)}]$$

$$Z_{out} = \frac{[R_{0(Device)}]}{A}$$

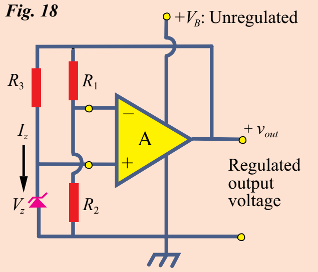
The output voltage "follows" the input voltage. It is used as a buffer amplifier with high-input/low-output impedance realization.

## Regulated Power Supply

- The zener diode offers a constant reference voltage ($V_Z$).
- Bias derived from the unregulated voltage ($V_B$) via potential division by $R_1$ and $R_2$ and the zener reference voltage are compared by an inverting amplifier to provide a stable output voltage.

$$v_{out} = V_Z\left(1+\frac{R_1}{R_2}\right) \text{ and } I_Z = \frac{(v_{out} - V_Z)}{R_3}$$

*Fig. 18*



# Unipolar Devices: Field-Effect Transistors (FETs)

## Definitions

- The **device current** is only determined by a type of current carrier (unipolar).
- The **device interior current** is controlled via the application of an electric field in the path of the current carriers.

## FET Types

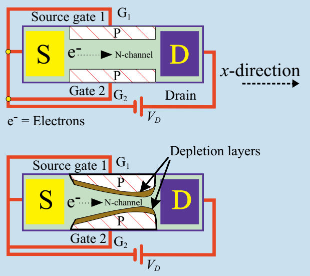
- **JFET (Junction Field-Effect Transistor):** In a JFET, the resistance of the current path is modulated via the application of bias voltages to **PN** junctions adjacent to it.
- **MOSFET (Metal-Oxide Semiconductor FET):** In a MOSFET, junctions are absent. The controlling electric field is applied *via* an insulating layer to regulate the resistance of a main conducting path.

## FET Operation Modes

- **Depletion-mode operation:** The controlling electric field decreases the number of carriers available for conduction.
- **Enhancement-mode operation:** Application of the electric field increases the majority-carrier density in the conducting regions of the transistor.

## JFETs: Device Operation

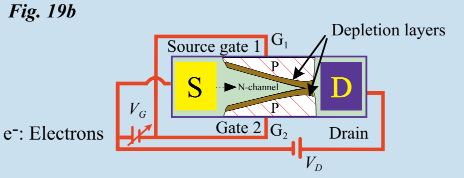
*Fig. 19a*



- Given the application of the voltage across **source (S)** to **drain (D)**, electrons flow from **S** to **D** (majority-carrier flow). The path between **S** to **D** exhibits ohmic resistance. Therefore, flow of the electron current causes a voltage drop, and the potential at any point along this path (***x***-direction) increases from source to drain (becoming more positive toward the drain end). The gates (tied together) are connected to the source, and thus the **N**-channel region and the regions of the **gate** form a reverse-biased **PN** junction.
- The extent of reverse bias progressively increases from source side to drain side. Correspondingly, the depletion layers formed are wider near the drain side as shown.
- Typically, the **P**-type gates ($G_1$ and $G_2$) are heavily doped relative to the **N**-channel region. Therefore, the channel exhibits (relatively) high resistance. Hence, the depletion layer widens predominantly into the channel region. Assume that $V_D$ increases. Thus, the depletion layer into the channel increasingly widens. Therefore, the two (top and bottom) depletion layers eventually meet each other. Hence, the channel is closed and does not permit the flow of electrons through it. This condition is termed as the **pinch-off**.

## Output Characteristics of JFETs

*Fig. 19b*



- Assume that an additional bias $V_G$ is applied between the gate and source terminals.
  - Assume that $V_G = 0$. In the absence of a drain current, the depletion layer is uniform along the channel. Increases in $V_D$ increase $I_D$. The corresponding voltage drop along the channel creates a wedge-shaped path due to the aforementioned reasons. Upon pinch-off, the drain current remains constant at a saturated value.
  - When $V_G$ is applied, this provides additional reverse bias. Therefore, pinch-off occurs at lower $V_D$ and the corresponding $V_{D(sat)}$ is also lower. Hence, the application of $V_G$ modulates the channel dimension and reduces $I_D$. This corresponds to a depletion-mode operation. The channel current decreases when the gate voltage increases.

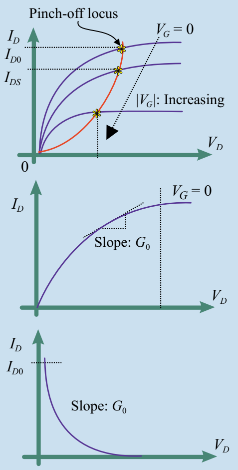
## Linear Operation of JFETs

- Assume that a channel is lightly doped relative to the gates (i.e., $N_{a(gate)} >> N_{d(channel)}$). ∴ Thickness of the depletion layer in the **N**-channel is $d_n \cong \left[2\varepsilon\frac{(V_0+V_G)}{eN_D}\right]^{\frac{1}{2}}$
- ∴ When $V_G$ changes, $d_n$ changes.
  - $V_0$: Contact potential; $N_a$ and $N_d$ correspond to acceptor and donor concentrations, respectively.
  - Σ: Permittivity of the channel
- Let $V_{P0}$ denote the value of $V_G$ at which pinch-off occurs. The corresponding change in $I_D = 0$. For $V_G < V_{P0}$,

$$I_D \approx G_0 1\left[-\left(\frac{V_G}{V_{P_0}}\right)^{\frac{1}{2}}\right]V_D,$$

where $G_0$ = **channel conductance** with zero bias ($V_G = 0$) condition:

*Fig. 20*



$$G_0 = (eN_d\mu_e) \times \frac{\text{Area of cross-section of the channel}}{\text{Length of the channel}}$$

- $e$: electronic charge
- $\mu_e$: electron mobility

## JFET Operation

Upon pinch-off:

$$I_{DS} = I_{D_0}\left[1-\frac{3V_G}{V_P}+2\left(\frac{V_G}{V_P}\right)^{\frac{3}{2}}\right]$$

Transfer characteristics:

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_G}\right|_{V_D} = -I_{D_0}\frac{3V_D}{V_P^2}\left[1-\frac{V_G}{V_P}\right]^{\frac{1}{2}}$$

$$g_m \triangleq \frac{\text{Mutual}}{\text{Transfer conductance}}$$

$$= \textbf{Max } g_m = g_m|_{V_G=0} = g_{m_0} = \frac{-3I_{D_0}}{V_P} = -G_0$$

= Conductance of the channel with zero bias

$$g_m \cong g_{m_0}\left[1-\left(\frac{V_G}{V_P}\right)^{\frac{1}{2}}\right]$$

# Unipolar Devices: MOSFETs

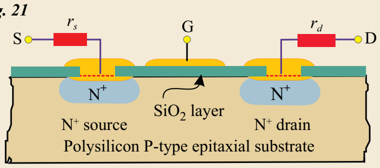
## Definitions

⇒ Induced-channel device/insulated-gate FET (IG FET)

- The gate is completely insulated from the semiconductor by a thin layer of $SiO_2$.
- The voltage applied at the gate induces a conducting channel within the semiconductor and modulates its conductivity.

### Enhancement-Type MOSFETs

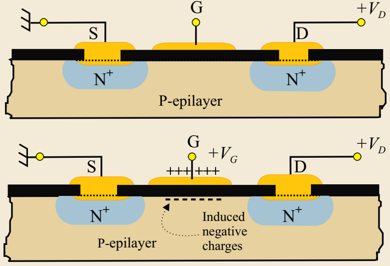
*Fig. 21*



$SiO_2$ ⇒ **100 to 300 A°** (thermally grown insulation layer)

## MOSFET Operation

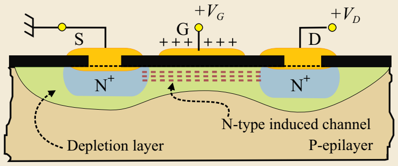
*Fig. 22*



- Assume that gate voltage is not applied. Then, **$N^+$P** junction at the source and **P$N^+$** junction at the drain are reverse biased. Thus, the drain current does not flow.
- Assume that a small **$+V_G$** is applied at the gate. The positive voltage at the top of the $SiO_2$ dielectric induces negative charges below the layer. The negative charges deplete the holes of the **P**-epilayer and expose negatively charged acceptor ions (i.e., a depletion layer is formed just below the gate as shown in *fig. 22*). A further increase in **$+V_G$** induces increasingly negative charges below the gate, thereby resulting in a significant accumulation of negative charges below the gate to form an induced layer of negative charges that constitutes a **"channel" (induced channel)** between the source and drain as shown in *fig. 23*.

*Fig. 23*

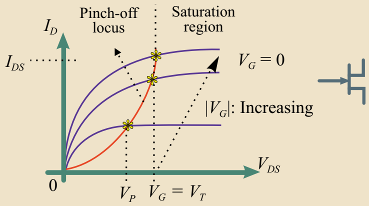
**N-Type Induced Channel**



- When the channel is induced between the **S** and **D**, the electrons flow through the channel, resulting in a drain current. Therefore, the induced channel constitutes an ohmic path. The conductivity of the channel is dependent on the magnitude of $V_G$. Thus, the channel conductivity is modulated via $V_G$. Therefore, increases in $V_G$ increase $I_D$. Thus, the device operates in enhancement mode.

## MOSFET Output Characteristics

*Fig. 24*



- **Analysis:** Let voltage at $x$ along the channel be $V(x)$.

$$I_D = \left(\frac{\mu_e C_g}{L^2}\right)\left(\frac{V_G - V_T - V_D}{2}\right)V_D \Rightarrow I_D \text{ versus } V_D \text{ is valid if}$$

$V_G - V(x) > V_T$.

**Note:** $L$: Channel length. At a given gate voltage $V_{G_1}$ with $V(x) = V_D$, the channel is turned open and the flow of charges along the channel is constant, i.e., at

$$V_D = V_{G_1} - V_T, \quad I_{ds} = \frac{\left(\frac{\mu_e C_g}{L^2}\right)(V_G - V_T)^2}{2}$$

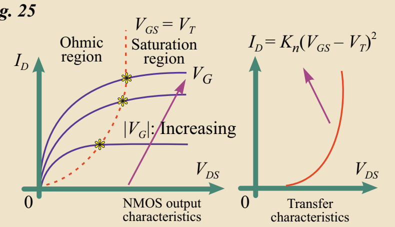
$$\left.\frac{\partial I_D}{\partial V_G}\right|_{V_D} \Rightarrow g_m = \mu_e C_g \frac{V_D}{L^2}$$

- ≜ Transconductant of the MOSFET

$$I_{DS} = I_D\Big|_{V_D = V_G - V_T} = \frac{\mu_e C_g}{2L^2}(V_G - V_T)^2 = g_m \frac{V_D}{2}$$

## V-I Characteristics of Enhancement-Type MOSFETs

*Fig. 25*



- **Ohmic region (triode region)**
  - $V_{DS} \le V_{GS} - V_T$ and the V-I characteristic is $I_D = K_n[2(V_{GS} - V_T)V_{DS} - V^2_{DS}]$, where:
    - ▫ $K_n = \frac{\mu_e \varepsilon_0 \varepsilon_{ox}}{2t_{ox}}\left(\frac{W}{L}\right) = \frac{\mu_e C_{ox}}{2}\left(\frac{W}{L}\right)$
    - ▫ $\mu_e$ = Surface mobility of electrons (= **800 cm²**/volt-sec [in Si])
    - ▫ $\varepsilon_0$ = Permittivity of free space (= **8.85 × $10^{-14}$ F/cm**)
    - ▫ $\varepsilon_{ox}$ = Dielectric constant of $SiO_2$ (≅ **4**)
    - ▫ $t_{ox}$ = Thickness of the oxide
    - ▫ $C_{ox}$ = Capacitance of the $SiO_2$ layer $\left(= \frac{\varepsilon_0 \varepsilon_{ox} LW}{t_{ox}}\right)$
  - Dividing locus between saturation and ohmic regions is given by substituting:

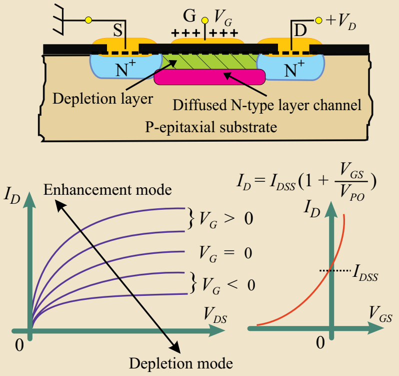
    $V_{DS} = (V_{GS} - V_T)$: $I_D = K_n V^2_{DS} = \frac{\mu_e C_{ox} W}{2L}(V^2_{DS})$
    - ▫ The locus is denoted by the dotted line in *fig. 25*.
- **Saturation region:** $V_{DS} \ge V_{GS} - V_T$, and current $I_D$ is approximately constant as shown in *fig. 25*. The transfer characteristic is obtained by replacing $V_{DS}$ by $V_{GS} - V_T$: $I_D = K_n(V_{GS} - V_T)^2$. A plot of the transfer characteristic is shown in *fig. 25*.
- **Cutoff region:** Here, $V_{GS} < V_T$, and thus $I_D$ = **0**. The device is *off* in the region and is used in switching applications in the mode.

## Diffused-Channel (Depletion-Type) MOSFETs

- A diffused-channel MOSFET can be operated as a depletion-mode and as an enhancement-mode device.
- The device exhibits a thin **N**-type layer with the same conductivity as a source or drain and is diffused below the gate.
- When the gate exhibits a small negative bias, the resulting positive charges in the diffused region decrease the depletion layer (channel conductance). Thus, negative bias on the gate enables depletion-mode operation.

*Fig. 26*

**Diffused-Channel MOSFET**

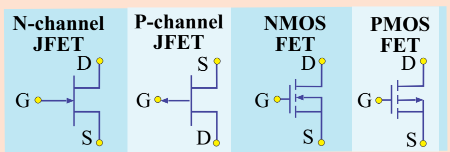


- When a positive bias is applied, more electrons are drawn into the channel, thereby increasing carrier population (i.e., channel conductance increases). This increases the flow of the current. Increases in $+V_G$ increase $I_D$ ⇒ *enhancement-mode operation*. The **V-I** characteristics indicate that circuit operations of diffused-channel MOSFETs are similar to those of JFETs.

# Small-Signal Equivalent Circuits & Frequency Response of FETs

Normal symbolic representations of the JFETs and the MOSFETs are shown in *fig. 27*.

*Fig. 27*



- A current in a FET is carried by majority carriers drifting under the effect of an electric field. Conversely, in the bipolar transistor, a current is transported via diffusing minority carriers. Drift velocities in semiconductors typically significantly exceed diffusion velocities, and thus carrier transit times are significantly lower in FETs than in bipolar transistors. Thus, FETs are expected to exhibit a significantly extended high-frequency range compared to bipolar devices.

*Fig. 28*

**Approximate Low-Frequency Equivalent Circuits**

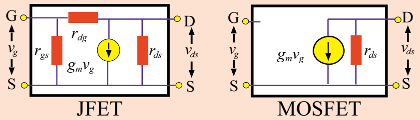
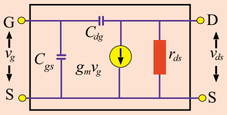


*Fig. 29*

**High-Frequency Equivalent Circuit of a JFET**



- A limitation to the high-frequency performance or the switching speed of a FET corresponds to the gate-channel capacitance, which must be charged via channel resistance. The resulting time constant determines the upper limit of the frequency response. The gain × bandwidth product (which can be derived from the equivalent circuit and corresponds to $\frac{g_m}{2\pi C_g}$) is normally considered as a *figure of merit* to indicate the high-frequency response of a specific device.

$\frac{g_m}{C_g} = \mu_e \frac{V_g - V_T}{L^2}$, where $C_g$ = total gate capacitance

## Common-Gate Amplifier

A common-gate (**CG**) FET amplifier circuit and its equivalent circuits are shown in *fig. 30*, p. 4.

$$A_v = \frac{v_0}{v_{in}} = \frac{(\mu + 1)R_L}{r_d + R_L} \cong g_m R_L \text{ for}$$

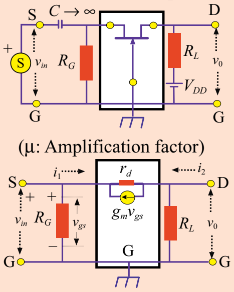
$$\mu = g_m r_d >> 1,\ r_d >> R_L$$

$$R_i = \frac{v_{in}}{i_1} = \frac{R_L + r_d}{\mu + 1} \cong \frac{1}{g_m} \text{ for } r_d >> R_L$$

$$R_0 = \frac{v_0}{i_2} = r_d + (\mu + 1)R_G \cong r_d + \mu R_G$$

**Note:** With respect to the **CG** configuration, the output resistance is extremely high and can be considered as infinite; the input resistance is relatively low. Voltage gain is dependent on $R_L$, and its maximum value is approximately μ. The **CG** configuration in FET corresponds to the counterpart of the **CB** configuration in BJTs.

*Fig. 30*
Common-Gate Amplifier

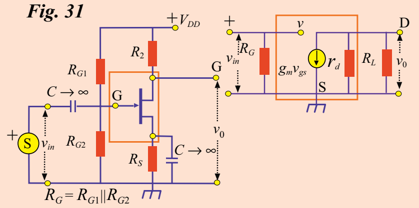


(μ: Amplification factor)

## Common-Source Amplifier

A common-source **(CS)** FET amplifier (with the DC biasing circuitry) and its small-signal equivalent circuit are shown in *fig. 31*.

*Fig. 31*



$$R_{in} \to \infty,\ R_0 = r_d, \text{ and } v_0 = -g_m(r_d \| R_L)v_{in}$$

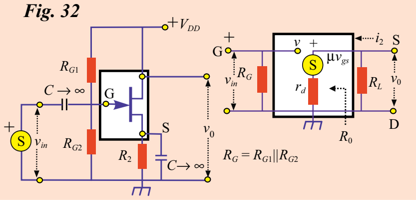
$$A_v = \frac{v_0}{v_{in}} = -g_m(r_d \| R_L) \cong -g_m R_L \text{ for } r_d >> R_L$$

$$\left(\frac{v_0}{v_{in}}\right)\max = -g_m r_d = \mu >> 1$$

## Common-Drain Amplifier

A common-drain **(CD)** FET amplifier (with the biasing circuitry) and its small-signal equivalent circuit are shown in *fig. 32*.

*Fig. 32*



$$R_{in} \to \infty$$

$$R_0 = \frac{v_0}{i_2} = \frac{r_d}{1+\mu} \cong \frac{r_d}{\mu} = \frac{1}{g_m} \text{ for } \mu >> 1$$

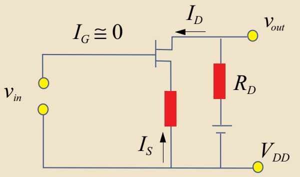
$$A_v = \frac{v_0}{v_{in}} = \frac{\mu R_L}{(1+\mu)R_L + r_d} \cong \frac{g_m R_L}{1 + g_m R_L}$$

With respect to $g_m R_L >> 1$, the voltage gain is close to unity. Thus, the **CD** configuration is termed as the **source follower (SF)** since the source voltage follows the input gate signal. The **CS** configuration in FET corresponds to the counterpart of the **CC** configuration in BJT.

# Summary on JFETs & MOSFETs

## N-Channel JFETs

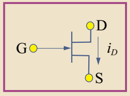
*Fig. 33*
Common-Source Amplifier



**Parameters**

| | |
|---|---|
| $V_T$ | – |
| $K$ | $\frac{I_{DSS}}{V_p^2}$ |
| $\lambda \cong \frac{1}{V_A}$ | + |
| $r_0$ | $\frac{\lvert V_A \rvert}{I_D}$ |
| $V_{DS}$ | + |

**Symbol**



$$v_{in} = V_{GS} - I_S R_S$$

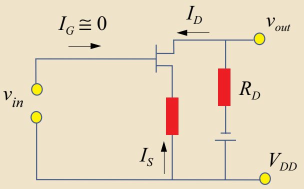
$$v_{out} = -V_D - I_D R_D = V_{DS} - I_S R_S$$

$$A_v = \frac{\Delta(V_{out})}{\Delta(V_{in})} = \frac{-R_0}{R_S + \frac{1}{g_m}}$$

- On-state: $v_{GS} > V_T$
- Saturation region:
  $v_{DS} \geq v_{GS} - V_T$ and $i_D = K(v_{GS} - V_T)^2(1 + \lambda V_{DS})$
- Triode region:
  $V_{DS} \geq V_{GS} - V_T$ and $i_D = K\left[2(v_{GS} - V_T)v_{DS} - v^2{}_{DS}\right]$
- $V_A$: A FET parameter

## P-Channel JFETs

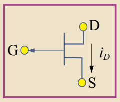
*Fig. 34*
Common-Source Amplifier



**Parameters**

| | |
|---|---|
| $V_T$ | + |
| $K$ | $\frac{I_{DSS}}{V_p^2}$ |
| $\lambda \cong \frac{1}{V_A}$ | – |
| $r_0$ | $\frac{\lvert V_A \rvert}{I_D}$ |
| $V_{DS}$ | – |

**Symbol**



$$V_{in} = V_{GS} - I_S R_S$$

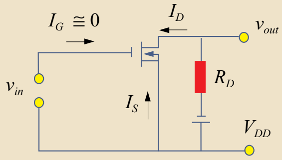
$$V_{out} = -V_{DD} - I_D R_D = V_{DS} - I_S R_S$$

$$A_v = \frac{\Delta(V_{out})}{\Delta(V_{in})} = \frac{-R_0}{R_S + \frac{1}{g_m}}$$

- On-state: $v_{GS} \leq V_T$
- Saturation region:
  $v_{DS} \leq v_{GS} - V_T$ and $i_D = K(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
- Triode region:
  $V_{DS} \geq V_{GS} - V_T$ and $i_D = K\left[2(v_{GS} - V_T)v_{DS} - v^2{}_{DS}\right]$

## N-Channel Depletion MOSFETs

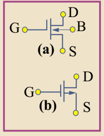
*Fig. 35*
Common-Source Amplifier



**Parameters**

| | |
|---|---|
| $V_T$ | – |
| $K$ | $\frac{\mu_n C_{OX} W}{2L}$ |
| Others | As for N-channel JFET |

**Symbol**



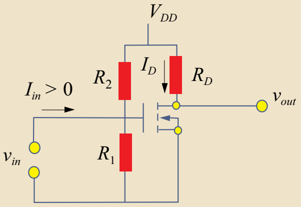
$$v_{in} = V_{GS} \text{ and } v_{out} = -V_{DD} - I_D R_D = V_{DS}$$

$$A_v = \frac{\Delta(V_{out})}{\Delta(V_{in})} \cong -g_m R_D$$

**(a)** Conventional
**(b)** When substrate/body "B" is connected to the source
**Note:** Different states and regions of operation: ⇒ Same as that for **N**-channel JFET

## N-Channel Enhancement MOSFETs

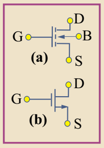
*Fig. 36*
Common-Source Amplifier



**Parameters**

| | |
|---|---|
| $V_T$ | + |
| Other parameters | As for N-channel depletion MOSFET |

**Symbol**



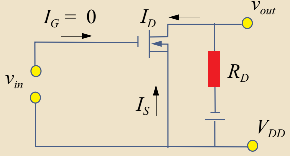
$$v_{in} = V_{GS} \text{ and } v_{out} = -V_{DD} - I_D R_D = V_{DS}$$

$$A_v = \frac{\Delta(V_{out})}{\Delta(V_{in})} \cong -g_m R_D$$

**(a)** Conventional
**(b)** When substrate/body "B" is connected to the source
**Note:** Different states and regions of operation: ⇒ Same as that for **N**-channel JFET

## P-Channel Depletion MOSFETs

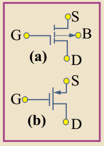
*Fig. 37*
Common-Source Amplifier



**Parameters**

| | |
|---|---|
| $V_T$ | + |
| $K$ | $\frac{\mu_p C_{ox} W}{2L}$ |

**Symbol**



$\mu_p$: Hole mobility

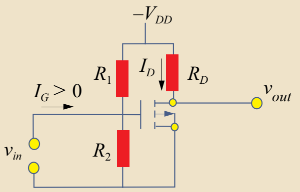
$$v_{in} = V_{GS} \text{ and } v_{out} = -V_{DD} - I_D R_D = V_{DS}$$

$$A_v = \frac{\Delta(V_{out})}{\Delta(V_{in})} \cong -g_m R_D$$

**(a)** Conventional
**(b)** When substrate/body "B" is connected to the source
**Note**: Different states and regions of operation: ⇒ Same as that for **N**-channel JFET

## P-Channel Enhancement MOSFETs

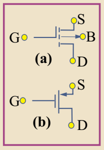
*Fig. 38*
Common-Source Amplifier



**Parameters**

| | |
|---|---|
| $V_T$ | – |
| Other parameters | As for P-channel depletion MOSFET |

**Symbol**



$$v_{in} = V_{GS} \text{ and } v_{out} = V_{DD} - I_D R_D = V_{DS}$$

$$A_v = \frac{\Delta(V_{out})}{\Delta(V_{in})} \cong -g_m R_D$$

**(a)** Conventional
**(b)** When substrate/body "B" is connected to the source
**Note:** Different states and regions of operation: ⇒ Same as that for **N**-channel JFET

## Summary on JFETs & MOSFETs (*continued*)

### Comparison of FET Amplifiers

| | CG | CS | CD(SF)* |
|---|---|---|---|
| $R_{in}$ | $\frac{1}{g_m}$ | $\infty$ | $\infty$ |
| $R_0$ | $\infty$ | $r_d$ | $\frac{1}{g_m}$ |
| $A_v = \frac{v_0}{v_{in}}$ | $g_m R_L$ | $-g_m R_L$ | $\frac{g_m R_L}{g_m R_L + 1}$ |

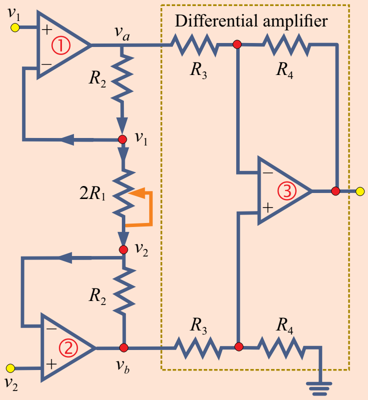
***SF:** Source follower

## Op-Amps Revisited

- **Instrumentation amplifier:** A high-performance differential amplifier with high-input impedance
  - $V_0 = -\left(\frac{R_4}{R_3}\right)\left(1+\frac{R_2}{R_1}\right)(V_1 - V_2)$
  - Input impedance presented at both inputs approaches infinity.
  - Output impedance of the differential amplifier approaches zero.
  - **Application:** To amplify differential signal(s) from transducers/sensors
  - $R_1$ can be adjusted to achieve null-offset.

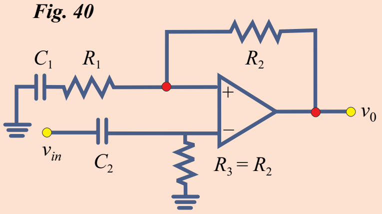
*Fig. 39*

**Common-Source Amplifier**



- **AC-coupled noninverting amplifier**
  - Capacitive coupling of an op-amp significantly decreases the DC offset.
  - Provision of $R_3$ is mandated to facilitate a continuous DC path for each of the input terminals.

*Fig. 40*



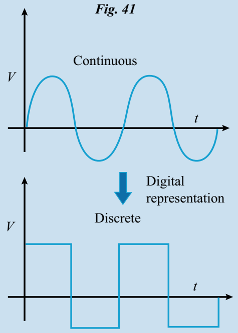
- A summary of op-amps:
  - Op-amps in practical circuits offer performance-matching theoretical estimations.
  - An op-amp consists of:
    - An inverting input terminal
    - A noninverting input terminal
    - An output terminal
    - Two power supply terminals + and –, with a common circuit ground
  - Ideally, an op-amp responds to the two inputs ($+v_{in1}$) and ($-v_{in2}$) to yield an output:
    - $V_0 = A(v_{in1} - v_{in2})$
    - $A$ is known as the open-loop gain, which is very large (ideally $A \Rightarrow \infty$; in practice, $A \sim 10^4$ to $10^6$).
  - An ideal op-amp exhibits an infinite input impedance (at both input terminals) and a zero-output impedance.
  - With negative feedback, the closed-loop gains are:
    - For an inverting input: $\frac{v_0}{v_{in1}} = \frac{R_2}{R_1}$
    - For a noninverting input: $\frac{v_0}{v_{in2}} = \left(1+\frac{R_2}{R_1}\right)$

## Digital Electronics

### Digital Representation

- Digital electronics involves discretizing a continuous signal value into a single value (i.e., a digital signal). *fig. 41* shows the digital representation of a continuous sine wave. The values of a sine wave are discretized as either 0 or $V_{peak}$ value of the sine wave.
- A digital signal offers advantages in terms of its immunity to noise. However, a digital signal can only transmit two values (e.g., 0 or 1, or false or true). Thus, this can result in loss of precision.
- **Bit:** A single value of either 0 or 1 is termed as a bit or a binary digit.
- Multiple-bit signals are transmitted over multiple wires. They are transmitted over a single wire via time-multiplexing multiple bits.
  - The two-level representation is termed as a binary representation.

*Fig. 41*



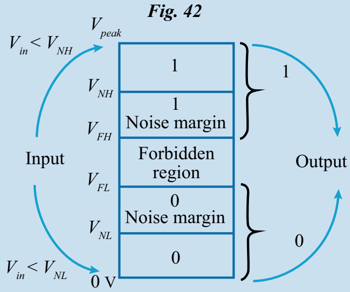
### Digital Circuits

- Digital circuits are constructed on the two-level representation of binary values wherein they only transmit 0 or 1. Digital signals are formed via discretizing voltage levels.
- Generally, **0 V** denotes a “low” or a logical “false” value, and $V_{peak}$ denotes a “high” or a logical “true” value. This convention can be changed for any circuit. Hence, it is arbitrary.

### Noise Immunity in Digital Circuits

- In digital devices, the analog voltage levels are mapped with digital signals such that the digital signal is immune to noise.
- As shown, the digital device accounts for noise using the forbidden region. High levels of noise are filtered via providing noise margins (i.e., if the input voltage is in the noise margin range, then it is not discarded).

*Fig. 42*



- In *fig. 42*, the signal voltage value between $V_{FH}$ and $V_{FL}$ is considered forbidden. The range can be adjusted by the device manufacturer. Hence, the device does not accept voltage in the forbidden region because it can lead to errors in determining a “high” or a “low” (i.e., 1 or 0).
- Noise margins are added outside the forbidden region to ensure that voltage values with noise in the acceptable noise margin range are not discarded.

### Boolean Logic & Digital Gates

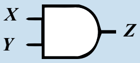
- Devices operate on Boolean logic wherein the input and output are in binary form (i.e., either 1 [high] or 0 [low]). The output of a device is based on the logic programmed in the device.
  - The logic for digital electronics is based on a few elementary logical operations that can be combined to program complicated logical operations. They are implemented in devices via digital gates. The list below specifies elementary logical operations or digital gates.

### Elementary Digital Gates: Seven Basic Logic Gates

The seven basic gates can be combined to form digital circuits, which can perform any type of logical operation. This list summarizes the seven basic gates with their equations and truth tables.

#### AND Gate

**Logic:** If $X$ is true AND $Y$ is true, then $Z$ is true, else $Z$ is false.

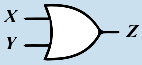


$Z = X \times Y = XY$

| $X$ | $Y$ | $Z$ (*out*) |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

#### OR Gate

**Logic:** If $X$ is true OR $Y$ is not true, then $Z$ is true, else $Z$ is false.

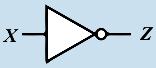


$Z = X + Y$

| $X$ | $Y$ | $Z$ (*out*) |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

#### NOT Gate

**Logic:** If $X$ is true, then $Z$ is false, else $Z$ is true.



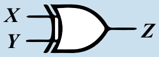
$Z = \overline{X}$

| $X$ | $Z$ (*out*) |
|---|---|
| 0 | 1 |
| 1 | 0 |

The bar on $X$ denotes inversion. Hence, if $X = \mathbf{1}$ (true), then $\overline{X} = \mathbf{0}$ (false).

#### XOR Gate

**Logic:** If $X$ or $Y$ are true, then $Z$ is true, else $Z$ is false if both $X$ and $Y$ are true or false.

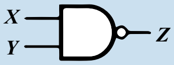


$Z = \overline{X}Y + X\overline{Y}$

| $X$ | $Y$ | $Z$ (*out*) |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

#### NAND Gate

**Logic:** Inversion of AND gate



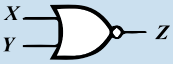
$Z = \overline{X \times Y}$

**Note:** $\overline{X \times Y} \neq \overline{X} \times \overline{Y}$

| $X$ | $Y$ | $Z$ (*out*) |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

#### NOR Gate

**Logic:** Inversion of OR gate



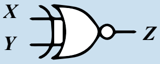
$Z = \overline{X + Y}$

**Note:** $\overline{X + Y} \neq \overline{X} + \overline{Y}$

| $X$ | $Y$ | $Z$ (*out*) |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

#### XNOR Gate

**Logic:** Complement of OR gate



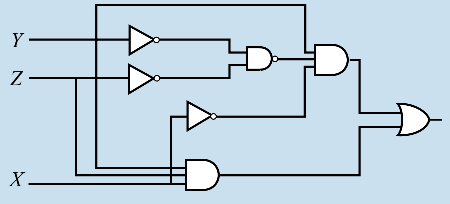
$Z = X \times Y + \overline{X} \times \overline{Y}$

| $X$ | $Y$ | $Z$ (*out*) |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## Combinational Gates

Several basic gates can be combined to form gates with a more involved logic (*fig. 43*). The representation of the combinational gates can be complicated. Hence, several Boolean algebra identities can aid in simplifying the logical expressions. This further simplifies the implementation of combinational gates.

***Fig. 43***



**Output:** $XYZ + X\overline{Y}(\overline{\overline{X}\,\overline{Z}})$

**EX:** The logical expression of the combinational gate shown in *fig. 43* is simplified via Boolean algebra identities.

The following identities are used for simplifying logical expressions.

**Boolean Algebra Identities**

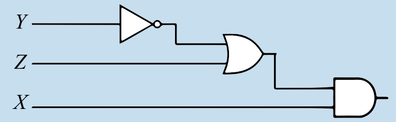
$$XYZ = (XY)Z = X(YZ)$$
$$X + Y + Z = (X + Y) + Z$$
$$XY = YX$$
$$X + Y = Y + X$$
$$X + YZ = (X + Y)(X + Z)$$
$$X(Y + Z) = XY + XZ$$
$$\overline{X + Y} = \overline{X}\,\overline{Y}$$
$$\overline{XY} = \overline{X} + \overline{Y}$$
$$XX = X$$
$$X + X = X$$
$$X + \overline{X} = 1$$
$$X\overline{X} = 0$$
$$X = \overline{\overline{X}}$$
$$X + XY = X$$
$$X + \overline{X}Y = X + Y$$
$$X \times 1 = X$$
$$X + 1 = 1$$
$$X + 0 = X$$
$$X \times 0 = 0$$

Hence, the Boolean expression for *fig. 43* can be simplified using the aforementioned identities.

$$\begin{aligned}
&XYZ + X\overline{Y}(\overline{\overline{X}\,\overline{Z}})\\
&= XYZ + X\overline{Y}(\overline{\overline{X}} + \overline{\overline{Z}})\\
&= XYZ + X\overline{Y}X + X\overline{Y}Z\\
&= XYZ + X\overline{Y} + X\overline{Y}Z\\
&= XZ(Y + \overline{Y}) + X\overline{Y}\\
&= XZ + X\overline{Y}\\
&= X(Z + \overline{Y})
\end{aligned}$$

Therefore, the combinational gate in *fig. 43* is simplified as shown in *fig. 44*.

***Fig. 44***



**Output:** $= X(Z + \overline{Y})$

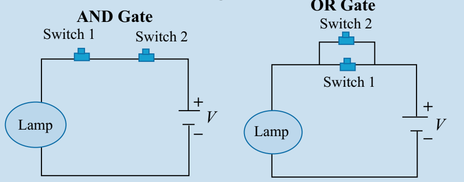
## Representation of Binary Numbers

- The decimal numbering system exhibits a base of 10. However, with respect to a binary numbering system, the base corresponds to 2. Hence, in order to represent a binary number $X_nX_{n-1}\ldots\ldots X_2X_1X_0$. As a decimal number, use the expression $\sum_{i=0}^{i=n} X_i 2^i$.
- An extra digit is added in front of the binary number to account for the sign of the number. Hence, typically the first digit is used to indicate the sign of the number. In this case, the above expression is modified as follows: $(-1)^{X_{n+1}} \sum_{i=0}^{i=n} X_i 2^i$.
- Thus, the aforementioned expression is used to represent a binary number $X_{n+1}X_nX_{n-1}\ldots\ldots X_2X_1X_0$ in decimal form.

## Implementing Logic Functions Using Switches

Switches are used to form logic gates. The two circuits shown below represent AND and OR gates.

***Fig. 45***



As shown in *fig. 45*, digital gates are easily implemented using switches. However, switches require mechanical pressure. Hence, MOSFETs constitute perfect candidates for switches. In MOSFETs, the G and S terminal is used as the input/control, and the D and S terminal is used as the output.

# Optoelectronics

Optoelectronic devices emit and modify light. The resistance of optoelectronic devices changes due to light, and thus they produce currents and voltages that are proportional to the intensity of the light.

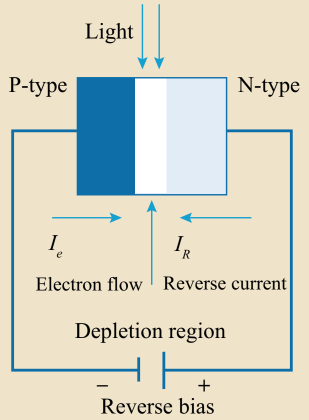
## Light-Emitting Diodes

- Charge-carrier recombination occurs at a forward-biased **PN** junction when electrons move from the **N**-side and recombine with holes on the **P**-side.
- Free electrons exhibit higher energy levels than holes do. A part of the energy is dissipated as heat or light during recombination.
- In translucent semiconductors, light is emitted, and thus the junction corresponds to a light source (i.e., a light-emitting diode).
- The number of holes created per second within a diffusion length of the transition region on the **N**-side corresponds to $AL_pg_{op}$. Furthermore, $AL_ng_{op}$ electrons are generated per second within $L_n$ of $x_{po}$, and $AWg_{op}$ carriers are generated within $W$. The resulting current due to the collection of the optically generated carriers in the junction is $I_{op} = qAg_{op}(L_p = L_n = W)$.

## Photodiodes & Solar Cells

- If a **PN** junction is reverse biased, then it leads to a small amount of reverse saturation current. This is because thermally generated holes and electrons move across the junction as minority charge carriers.
- Increases in the junction temperature increase the number of hole-electron pairs that are generated. Thus, this increases the reverse current. The same effect occurs if the junction is illuminated as shown in *Fig. 46*.

***Fig. 46***



Solar cells are essentially large photodiodes that are designed to generate maximum current from light energy. This is achieved by designing a solar cell with a large area junction located near the surface of the device.

# Integrated Circuits

## Complementary Metal-Oxide Semiconductors

- Modern circuits are integrated on a single layer of a semiconductor material and are commonly referred to as integrated circuits.
  - An **integrated circuit** is composed of a set of circuits. A **complementary metal-oxide semiconductor (CMOS)** is a technology used to construct modern integrated circuits including **microcontrollers** and **microprocessors**.
- In CMOS, both **P**-type and **N**-type transistors are used for logic gates. In this technology, the same signal is used to turn ON a transistor of one type and turn OFF a transistor of another type.
  - This allows for the use of simple switches such as MOSFETs. Thus, CMOSs are composed of an array of MOSFETs.

## Charge-Coupled Devices

- A **charge-coupled device (CCD)** is a broadly used integrated device. This is a dynamic device that moves a charge along a predetermined path under the control of clock pulses. The charge is moved from within the device to an area where the charge can be manipulated (i.e., converted to a digital value). This is achieved via individually "shifting" signals between stages within the device.
  - The modern digital camera is one of the most important applications of CCDs.

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